SUBSTITUTE SPECIFICATION

BUMPLESS FLIP CHIP ASSEMBLY WITH SOLDER VIA

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is continuation of U.S. application number 09/465,024 filed on December 16, 1999, which is an application filed in accordance with 35 U.S.C. §119 and claims the benefit of earlier filed Singapore application number 9804817-6 filed on December 17, 1998.

1. Field of the Invention

This invention relates generally to a semiconductor device assembly, and in particular, relates to a connection of integrated circuit (IC) chip or chips to substrate circuitry, printed circuit board, and interconnect components.

2. Background of the Invention

Recent developments of semiconductor packaging suggest an increasingly critical role of the technology. New demands are coming from requirements for more leads per chip and hence smaller input/output terminal pad pitch, shrinking die and package footprints, and higher operational frequencies that generate more heat, thus requiring advanced heat dissipation designs. All of these considerations must be met and, as usual, placed in addition to the cost that packaging adds to the overall semiconductor manufacturing costs.

Conventionally, there are three predominant chip-level connection technologies in use for integrated circuits, namely wire bonding, tape automated bonding (TAB) and flip chip (FC) to electrically or mechanically connect integrated circuits to leadframe or substrate circuitry. Wire bonding has been the far most broadly applied technique in the semiconductor industry because of its maturity and cost effectiveness. However, this process can be performed only one wire bond at a time between the semiconductor chip's bonding pads and the appropriate interconnect points. Furthermore, because of the ever increasing operational frequency of the device, the length of the interconnects needs to be shorter to minimize inductive noise in power and ground, and also to minimize crosstalk between the signal leads. An example of such a method is disclosed in U.S. Pat. No. 5,397,921 issued to Karnezos.

Flip chip technology is characterized by mounting of the unpackaged semiconductor chip with the active side facing down to an interconnect substrate through contact anchors such as solder, gold or organic conductive adhesive bumps. The major

advantage of flip chip technology is the short interconnects which can, therefore, handle high speed or high frequency signals. There are essentially no parasitic elements, such as inductance. Not only is the signal propagation delay slashed, but much of the waveform distortion is also eliminated. Flip chip also allows an array interconnecting layout that provides more I/O than a perimeter interconnect with the same die size. Furthermore, it requires minimal mounting area and weight which results in overall cost saving since no extra packaging and less circuit board space is used. An example of such a method is disclosed in U.S. Pat. No. 5,261,593 issued to Casson et al.

While flip chip technology has tremendous advantages over wire bonding, its cost and technical limitations are significant. First of all, prior art flip chip technology must confront the challenge of having to form protruded contact anchors or bumps to serve as electrical connections between the integrated circuit chip and substrate circuitry. Examples of such an approach are disclosed in U.S. Pat. No. 5,803,340 issued to Yeh et al. and U.S. Pat. No. 5,736,456 issued to Akram. These approaches typically include a very costly vacuum process to deposit an intermediate under-bump layer that serves as an adhesive and diffusion barrier. This barrier layer is typically composed of a film stack that can be in the structure of chromium/copper/gold. Bumping materials such as solder are subsequently deposited onto this intermediate layer through evaporation, sputtering, electroplating, solder jetting or paste printing methods followed by a reflow step to form the solder contacts. Although evaporation and sputtering can potentially offer high density bumps, these processes need very tight control and normally result in poor yield. As a result, a conventional flip chip assembly is not only very costly but also suffers from very serious reliability problems and a high fatality ratio.

Techniques for fabricating the intermediate under-bump barrier layer as well as the bump material utilizing electroless plating are also known in the prior art. An example of such a method is described in the U.S. Pat. No. 5,583,073 issued to Lin et al. Although the electroless technique provides an economical, simple and effective method for providing an under-bump barrier layer, contacting material such as solder or adhesive is still required for assembling. Solder dipping or screen printing of solder paste onto these bumps has been explored but has been met with very limited success due to lack of solder bridging control and non-uniform deposition of solder on the metal bumps. This process also suffers from poor process control as input/output terminal pad spacing gets smaller.

In view of the limitations of currently available integrated circuit assembling methods, a high performance, reliable and economical device and method that can effectively interconnect integrated circuits to the external circuitry would be greatly desirable.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a flip chip assembly to address high density, low cost and high performance requirements of semiconductor packaging. The device and method of the present invention involve the bonding of substrate circuitry to a semiconductor device through the reflowing of pre-deposited solder to connect via apertures or holes of the substrate to terminal pads of the semiconductor device without the need for conventional bumps, bonding wire, or other media.

More specifically, the present invention relates to a chip assembly that includes a single or multi-layered substrate of which circuitry is connected to the input/output terminal pads of the IC chip through solder reflow in the via holes. The solder deposition techniques include electrolytic plating, electroless (chemical) plating, wave soldering, meniscus coating and solder printing.

In summary, using soldering material directly reflowed between a via hole and a terminal pad can effectively connect an IC chip and dielectric substrate circuitry without external bumps or wires. This approach allows a reliable, low profile, high performance and low cost assembly to be achieved. In particular, a small via hole formed by laser drilling or other techniques allows a very fine pitch terminal pad to be interconnected, which can significantly enhance the capability of packaging future high I/O semiconductor chips.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a fragmented partial sectional side elevational view of a substrate before plating the via hole with solder.

Figure 1B is a fragmented partial sectional side elevational view of the substrate of the type shown in Figure 1A after plating the via hole with solder.

Figure 1C is a fragmented partial sectional side elevational view of a semiconductor chip having a terminal pad.

Figure 1D is a fragmented partial sectional side elevational view of a chip assembly after a semiconductor chip of the type shown in Figure 1C has been attached to a

substrate of the type shown in Figure 1B.

Figure 1E is a fragmented partial sectional side elevational view of the chip assembly of the type shown in Figure 1D after a solder reflow process.

DETAILED DESCRIPTION OF THE INVENTION

The bumpless flip chip assembly of the present invention includes a rigid or flexible dielectric substrate having a plurality of electrically conductive circuitry traces and a plurality of via apertures or holes. The conductive traces on the surface of the substrate extend into the via holes through the conductive material deposited on the via hole walls. This plated through-hole (PTH) material such as plated copper, gold, nickel, titanium or palladium provides a conductive base for solder deposition or solder wetting. Soldering material such as tin-lead alloy or lead-free solder is pre-deposited in the via hole or on the terminal pad. This readily available solder serves as the joint material after the substrate is attached to the semiconductor chip. The orientation of the attachment between the chip and substrate circuitry ensures that at least one of the via holes in the dielectric substrate is aligned with a terminal pad.

After alignment, the IC chip is brought in contact with the dielectric substrate through an adhesive film or paste, or mechanical techniques such as mechanical clamping. This soft or proximity contact ensures that the pre-deposited soldering material is able to reflow into the via hole as well as onto the terminal pad when it is molten. Heat, which serves to activate the flux and bring the solder to its melting point, is used to effect the metallurgical bonding. This re-flow process results in a solder joint which electrically and physically connects the via hole and IC pad. This not only assures a very cost effective and simple process, but also provides a compliant joint with significant stress release which results in a very reliable connection between the substrate circuitry and IC chip.

As defined herein, the preferred embodiment is particularly directed to the bonding of an integrated circuit (IC) chip to a flexible circuitized substrate, or to a more rigid, circuitized substrate, a particular example of the latter being a printed circuit board. It is to be understood, however, that the invention is not limited to the attachment to printed circuit boards, in that other circuitized substrates, including known plastic and ceramic substrates, may be employed. Typically, an organic-type substrate is preferable for lower cost and superior dielectric property whereas an inorganic-type substrate is preferable when high thermal dissipation and matched coefficient of expansion are desired. The term

"substrate" as used herein is defined as at least one layer of dielectric material having at least one conductive layer thereon. Printed circuit boards of similar type are well known in the electronics industry, as well as the processes for making the same, and therefore, further definition is not believed to be necessary. Such structures may include many more electrically conductive layers than those depicted in FIGS. 1A through 1E, depending on the desired operational characteristics. As is known, such electrically conductive layers may function as signal, power, and/or ground layers.

In one embodiment of the invention, the solder pre-deposition is in the via hole. In this embodiment, the via holes are first metallized with a base metal by a conventional plated through hole (PTH) technique followed by solder deposition. Solder deposition techniques include electroplating, electroless plating, wave soldering, meniscus solder coating, solder paste printing and dispensing to accomplish the pre-coating of solder material onto the metallized hole wall. It is understood that the particular solder or solder paste and methods of dispensing depicted herein are not meant to limit the invention.

In another embodiment of the invention, the solder pre-deposition is on the IC terminal pad. In this method, a barrier layer over-coated on an aluminum pad before solder deposition is preferred. This is to provide a good solder wetting surface and protect the aluminum surface against leaching, oxidation or degradation resulting from heat and soldering contact. This coating can be accomplished by sputtering a stake of thin film or by wet chemical direct plating of electroless nickel and immersion gold. For copper terminal pads, the pre-treatment may not be necessary when the surface is free of oxide and contamination.

The via holes of the substrate can be formed by various techniques including mechanical drilling, punching, plasma etching or laser drilling. They are formed in the substrate before or after the circuitry patterning depending on the various fabrication processes. The via holes are formed at locations that can be aligned with and expose input/output terminal pads of the semiconductor chip or chips that are subsequently mounted on the side of the substrate opposite the side where the electrical circuitry is formed.

A preferred application of heat to reflow pre-deposited solder is by a convection oven. Alternatively, the heat may be applied by a laser to effect solder reflow and bonding to the IC terminal pads which are in the vicinity of the via holes. Another example of such

an approach is an infrared (IR) continuous belt reflow oven. Alternatively, hot nitrogen gas may be directed onto the solder members of the assembly. It is understood that the particular re-flow techniques depicted above are not meant to limit the invention, in that it is also possible to reflow the solder using a vapor phase reflow system.

If the finished product is, for instance, a ball grid array package, solder balls will normally be placed on the specific traces on the surface of the dielectric substrate. This finished package can be connected to a printed circuit board by reflowing the solder balls to form an attachment to the conductors of the printed circuit board.

FIGS. 1A to 1E are diagrammatic cross-sectional views showing steps involved in the manufacturing of an integrated circuit assembly by pre-depositing solder in the substrate via hole and re-flowing the solder to connect the terminal pad.

Referring initially to FIG. 1A, a substrate 101 having a plurality of electrically conductive circuitry traces 102 partially covered by the solder mask 103 is shown. The traces 102 on the substrate 101 extend into a plurality of via holes 104 by a thin layer of plated through-hole copper 105 deposited on the via hole walls.

FIG. 1B shows the substrate 101 immersed in a solder plating solution and a layer of solder 106 is electroplated on the metallized via hole wall as well as on the solder opening site.

FIG. 1C shows an integrated circuit chip 107 having various types of transistors, wires and the like (not shown), which has a plurality of exposed input/output terminal pads 108. These pads 108 are formed with a stake of thin film 109 in the structure of titanium (500 Angstroms)/nickel (700 Angstroms)/gold (1000 Angstroms) to serve as the barrier and adhesive layer. Passivation is disposed on chip 107 outside pads 108.

FIG. 1D shows IC chip 107 securely attached to the substrate 101 by adhesive paste ABLESTIK "ABLEBOND 961-2" 110 to form an assembly 111. The orientation of the attachment is arranged in such a manner that a specific terminal pad 108 of the integrated circuit chip 107 is in contact with the solder 106 inside a specific via hole 104. The via hole 104 serves as an electrically connecting channel for the respective trace 102 of the substrate 101.

FIG. 1E shows the input/output terminal pad 108 firmly joined together with a specific via hole 104 by solder joint 112 to become an integral part after the assembly 111 is placed in an oven that causes solder 106 to reflow. This simultaneously-reflowed joint

112 provides an effective electrical and mechanical connection between IC chip 107 and substrate 101. The soldering material 113 deposited in the solder mask opening serves as the contacting material for the next level assembly.

Though only one integrated circuit chip 107 is shown, it is to be understood that additional integrated circuit chips, as well as passive components such as resistors or capacitors, can also be mounted on the substrate 101.

Likewise, it is to be understood that many solder systems including lead-free ones can also be applied and serve the connection purpose.

The present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The presently disclosed embodiments are, therefore, to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are, therefore, to be embraced therein.

What is claimed is: